In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 9, 40 and 41 without prejudice.

1. (Previously Presented) A computer system comprising:

a central processing unit (CPU); and

a cache memory, coupled to the CPU, having a plurality of compressible cache lines to store additional data; and

a cache controller to perform lookup operations of the cache memory, the cache controller having an array of tag entries corresponding to each of the plurality of cache lines, each tag entry including:

address tag bits corresponding to a cache line address;

one or more compression encoding bits indicating whether a corresponding cache line is compressed; and

one or more companion encoding bits indicating which companion lines are stored in a common cache set, wherein if the compression bit indicates the cache line is compressed the companion bit is disregarded and if the compression bit indicates the cache line is not compressed the companion bit is compared with a tag.

2. (Cancelled)

3. (Original) The computer system of claim 1 wherein the cache controller is included within the CPU.

4. (Cancelled)

5. (Previously Presented) The computer system of claim 1 wherein the cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed.

6. (Cancelled)

7. (Original) The computer system of claim 5 wherein the companion lines are adjacent memory lines.

8. (Previously Presented) The computer system of claim 1 wherein the companion encoding bits are used as a compression format bit to select between different compression algorithms.

9. (Cancelled)

10. (Previously Presented) The computer system of claim 1 wherein the cache controller further comprises set and way selection logic to select a cache line.

11. (Previously Presented) The computer system of claim 10 wherein the set and way selection logic comprises tag comparison logic to compare the cache line address to the address tag bits.

12. (Original) The computer system of claim 11 wherein the tag comparison logic ignores the one or more companion encoding bits within the address if the one or more compression encoding bits indicate that the cache line is compressed.

13. (Previously Presented) The computer system of claim 11 wherein the tag comparison logic compares ~~the~~ one or more companion bits within the address with the one or more companion encoding bits within the tag if the compression encoding bits indicate that the cache line is not compressed.

14. (Original) The computer system of claim 10 wherein the cache controller further comprises compression logic to compress a cache line.

15. (Original) The computer system of claim 14 wherein the compression logic compresses cache lines via a dictionary based compression algorithm.

16. (Original) The computer system of claim 14 wherein the compression logic compresses cache lines via a sign-bit compression algorithm.

17. (Original) The computer system of claim 14 wherein the compression logic determines when a cache line is to be compressed.

18. (Original) The computer system of claim 17 wherein the compression logic compresses a cache line based upon opportunistic compression.

19. (Original) The computer system of claim 17 wherein the compression logic compresses a cache line based upon prefetch compression.

20. (Original) The computer system of claim 17 wherein the compression logic compresses a cache line based upon victim compression.

21. (Original) The computer system of claim 14 wherein the cache controller further comprises byte selection logic to select addressed datum within a cache line.

22. (Original) The computer system of claim 21 wherein the byte selection logic comprises:

a decompressor to decompress a selected cache line;

an input multiplexer to select between a decompressed cache line and an un-decompressed cache line; and

an output multiplexer to select between companion lines in the uncompressed cache line.

23. (Previously Presented) A cache controller comprising:

compression logic to compress lines within a cache memory device; and

an array of tag entries corresponding to each of a plurality of cache lines, each tag entry including:

address tag bits corresponding to a cache line address;

one or more compression encoding bits indicating whether a corresponding cache line is compressed; and

one or more companion encoding bits indicating which companion lines are stored in a common cache set, wherein if the compression bit indicates the cache line is compressed the companion bit is disregarded and if the compression bit indicates the cache line is not compressed the companion bit is compared with a tag.

24. (Previously Presented) The cache controller of claim 23 further comprising set and way logic to select from a plurality of cache lines.

25. (Previously Presented) The cache controller of claim 23 ~~24~~ wherein a single cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed.

26. (Cancelled)

27. (Previously Presented) The cache controller of claim 24 wherein the set and way selection logic comprises tag comparison logic to compare ~~a~~ the cache line address to the address tag bits.

28. (Previously Presented) The cache controller of claim 27 wherein the tag comparison logic ignores the one or more companion encoding bits within the address if the one or more compression encoding bits indicate that the cache line is compressed.

29. (Previously Presented) The cache controller of claim 28 wherein the tag comparison logic compares one or more companion bits within the address with the one

or more companion encoding bits within the tag if the compression encoding bits indicates that the cache line is not compressed.

30. (Original) The cache controller of claim 23 wherein the compression logic compresses cache lines via a dictionary based compression algorithm.

31. (Original) The cache controller of claim 23 wherein the compression logic compresses cache lines via a sign-bit compression algorithm.

32. (Original) The cache controller of claim 23 wherein the compression logic determines when a cache line is to be compressed.

33. (Original) The cache controller of claim 23 wherein the cache controller further comprises byte selection logic to select addressed datum within a cache line.

34. (Original) The cache controller of claim 33 wherein the byte selection logic comprises:

a decompressor to decompress a selected cache line;

an input multiplexer to select between a decompressed cache line and an un-decompressed cache line; and

an output multiplexer to select between companion lines in the uncompressed cache line.

35. (Previously Presented) A method comprising:

analyzing a tag associated with a first cache line in a tag array to determine if the first cache line is compressed;

analyzing one or more companion encoding bits if the first cache line is not compressed; and

disregarding the one or more companion encoding bits if the first cache line is compressed.

36. (Previously Presented) The method of claim 35 wherein compressing the first cache line comprises storing data from a second cache line within the first cache line.

37. (Previously Presented) The method of claim 35 further comprising determining if a first cache line within a cache memory device is to be compressed.

38. (Previously Presented) The method of claim 37 further comprising compressing the first cache line.

39. (Cancelled)

40. (Cancelled)

41. (Cancelled)

42. (Previously Presented) A computer system comprising:

a central processing unit (CPU);

a cache memory, coupled to the CPU, having a plurality of compressible cache lines to store additional data;

a cache controller to perform lookup operations of the cache memory, the cache controller having an array of tag entries corresponding to each of the plurality of cache lines, each tag entry including:

address tag bits corresponding to a cache line address;

one or more compression encoding bits indicating whether a corresponding cache line is compressed; and

one or more companion encoding bits indicating which companion lines are stored in a common cache set, wherein if the compression bit indicates the cache line is compressed the companion bit is disregarded and if the compression bit indicates the cache line is not compressed the companion bit is compared with a tag;

a chipset coupled to the CPU; and

a main memory.

43. (Cancelled)

44. (Previously Presented) The computer system of claim 42 wherein the cache controller is included within the CPU.

45. (Previously Presented) The computer system of claim 42 wherein the cache controller is included within the chipset.

46. (Cancelled)

47. (Previously Presented) The computer system of claim 42 wherein a single cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed.